

Design Verity

VERITY-CPU FEATURES

Verity-Grand Master

Targeted instruction generation
Formal analysis of RTL
Exception handling,
OS sequence handling,
Instruction sequence filtering
Coverage analysis

Verity-Brisic

Biased random
User defined templates
User defined parameters
Undefined value support
Loop and branch handling
Exception handling
Instruction sequence filtering
MMU support
Coverage analysis

Verity-Cover

Coverage directed
Instruction permutation coverage
Instruction sequence coverage

Experience The Power of Formal Validation

Is your CPU design true to specification? Veritable's Design Verity software offers high performance, high capacity design validation solutions that significantly reduce the time to check.

Verity-CPU combines the practicality of simulation with the power of formal analysis

Design Verity-CPU, the Design Verity processor instruction stream generator, is an innovative formal validation tool that simplifies and speeds up design verification of CPUs. Verity-CPU combines the ease-of-use methodology of traditional biased random instruction stream generation tools and the power of formal analysis technology into a single solution, putting powerful CPU verification capability at your fingertips.

Verity-CPU comprises three innovative instruction stream generation modules:

Verity-Grand Master

Performs formal analysis of RTL and generates targeted instruction streams

Verity-Brisic

Generates biased-random instruction streams

Verity-Cover

Generates coverage directed instruction sequences

Verity-Grand Master generates targeted instruction streams that detect hard to catch bugs

Verity-Grand Master quickly analyzes your RTL design code and automatically generates instruction streams targeted at particular areas of your design. Verity-Grand Master's powerful analysis capability results in the detection of hard to detect bugs that are unlikely to be caught using random instruction sequences. One example of the type of bug that Verity-Grand Master has found was a micro-architectural bug in the pipeline control unit of a 500 MHz CPU. Detecting this bug required the generation of a specific sequence of instructions that set and used particular flags. This micro-architectural design bug had escaped detection despite many months of biased-random and directed testing but Verity-Grand Master's targeting technology enabled it to quickly generate several test cases that uncovered this bug.



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“Veritable's formal validation tools offer a promising way of increasing confidence that complex high performance CPU designs function according to their specification. Veritable's Design Verity software is an important part of our verification flow and has detected many issues. Just a few weeks from planned tape-out on a 500 MHz pipeline CPU, the Design Verity software detected a late stage architectural bug that had been present in the design for many months but had escaped detection by other methods.”

– Yukio Sakaguchi, Senior Vice President, Arcadia Design Systems, Inc.

Verity-BrisC generates user controlled biased-random instruction streams

Verity-BrisC offers powerful biased-random instruction stream generation capability based on user templates. You control the types of sequences generated by Verity-BrisC by specifying parameters such as weights, sequence templates and filters in a configuration file. Verity-BrisC uses this configuration and an instruction set information file to automatically generate sets of biased random instruction sequences. Verity-BrisC has detected dozens and dozens of bugs including several bugs in a CPU that had already taped out.

Verity-Cover increases design confidence

Verity-Cover augments Verity-Grand Master and Verity-BrisC by performing coverage directed test generation targeted at improving instruction permutation and instruction sequence coverage. Verity-Cover increases your confidence that you have covered your design sufficiently.

Experience the power of formal validation

Veritable's Verity-CPU combines the ease of use methodology of traditional random instruction generation tools with the power of formal analysis technology into a single high performance, high capacity CPU verification solution. With Verity-CPU, you get a unique combination of formal analysis

and biased-random instruction stream generation technology that gives you the most comprehensive and powerful CPU verification capability available.

Experience the power of formal validation now at <http://www.veritable.com>.

HDL Support

Verity-CPU 1.0 supports Verilog designs. VHDL support will be available in Q1 2002.

Platforms Supported

Verity-CPU supports Unix/Solaris and Windows NT/98.

Availability

Verity-CPU 1.0 is available now in a solutions plus services package.



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